	Document # **LAT-TD-00232**	Date Effective 5/30/01
	Prepared by(s) Robert Johnson Masa Hirayama	Supersedes None
GLAST LAT TECHNICAL DOCUMENT	Subsystem/Office Tracker Subsystem	
Document Title Noise Analysis of the LAT Tracker Amplifier		

Gamma-ray Large Area Space Telescope
(GLAST)
Large Area Telescope (LAT)
Noise Analysis of the LAT Tracker Amplifier

1 Abstract

Transient and noise simulation results are presented for the Tracker front-end amplifier in order to evaluate the expected signal-to-noise. The results are compared with measurements made on the "Top5" prototype.

2 The Amplifier Design

Figures 6, 7, 8, 9, 10, 11, and 12 show the schematic for the amplifier that was simulated. The reset circuit (ARESET5) was disabled, and the simulations were made with a high threshold such that the comparator never fired. Three configurations were simulated:

1. Standard, as shown in the schematic. This represents the originally intended operation of the test chip.

2. Improved comparator. MP32 in the bias circuit is changed from M=1 to M=5 and the coupling capacitor C5 in the comparator is doubled in size. This is the configuration of the coupling in the 64-channel GTFE prototype submission.
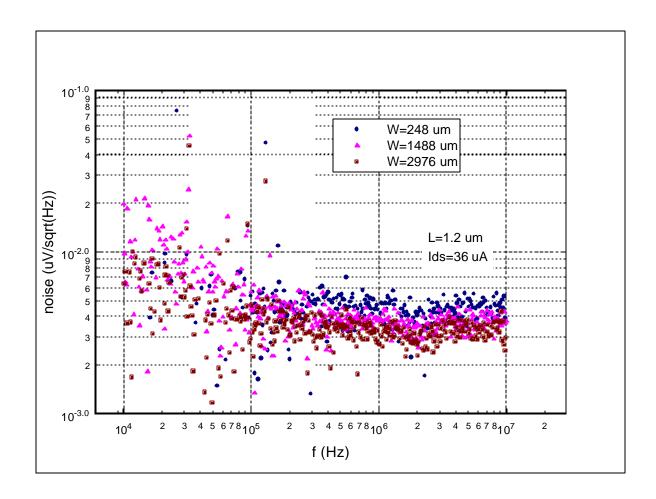

Figure 1. Measured transistor noise spectra, showing the dependence on transistor width.

3. Short time constant: as in configuration 1, but with the current source setting IBIAS increased from 2.5 µA to 5.0 µA, and a 6 MΩ resistor added from ILOW to ground. This moves the peaking time into the range desired for triggering of the calorimeter and shortens the time-over-threshold to keep the Tracker trigger dead time more in line with that of the calorimeter.

4. Improved comparator and short time constant: MP32 in the bias circuit is changed from M=1 to M=5, the coupling capacitor C5 in the comparator is doubled in size, and the transistor MP21 in the comparator is shorted out (equivalently, its gate is disconnected from the output and grounded). This reduces the large (40%) loss of signal/noise caused by this AC coupling in the Top5 test chip and also prevents the comparator from hanging in the high state. Note that the full-scale GTFE64d chip submitted to MOSIS at the end of April 2001 has the improved coupling but does not have MP21 shorted out.

The test chip was implemented in the Agilent/HP 0.5 µm AMOS14TB CMOS process. We used the BSIM3 V3.1 Spice models (Level 7 in PSpice) derived by MOSIS for the T0CN run on this process.

3   Spice Simulation

The simulations were done with the bias current of the input FET set at 37 µA and with the amplifier input loaded by a 47 pF capacitor to ground. This loading simulates what we expect from the detector (about 1.3 pF/cm).[1] The power (VDD) was set to 2.5 V. First, a simulation was done with the input FET standing alone and biased with this current, in order to see the noise contribution built into the model (which included only white noise). The result was that the transistor noise was predicted to be 3.9 nV/$\sqrt{\text{Hz}}$. This compares reasonably well with our measurements for a W=1488 µm, L=1.2 µm transistor, as shown in Figure 1 and Figure 2, to the extent that the measured noise around 200 kHz can be read from the scatter of data points.

Next, a transient simulation was done for each case with 0.92 fC of input charge, and the peak amplitude was noted at the output of the shaper and at the input of the comparator (i.e. after the AC coupling). The peaking time was also noted. Finally, an AC noise simulation was done, and the output noise spectrum was integrated. Comparing the noise simulation with the transient simulation, we extract the signal-to-noise, expressed as an equivalent noise charge (ENC) at the amplifier input. Note the loss of signal-to-noise due to the AC coupling to the comparator.

---

[1] Such a simple representation of the detector, however, does not include other sources of noise, such as noise from adjacent channels feeding through via the interstrip capacitance or shot noise from the detector leakage current.
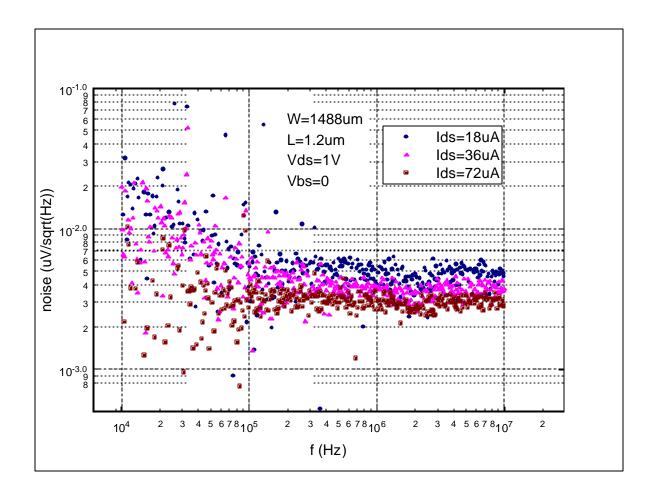
Figure 2. Measured transistor noise spectra, showing the dependence on drain current.

4   Top3 Test-Chip Measurements

The "Top3" test chip included three isolated FETs of the same length (1.2 µm) as the input FET in the amplifiers and three widths: 248 µm, 1488 µm, and 2976 µm. The input FETs in the amplifiers have width 1488 µm. The transistor noise was measured with a drain-source voltage of 1.0 V and with the well voltage equal to the source voltage. A custom amplifier was used to amplify the noise at the FET drain before inputting it into a spectrum analyzer. A network analyzer was used to measure the gain at each frequency point, to translate the noise to the FET gate input. The background noise was also measured with the FET drain current zeroed and was subtracted from the measured FET noise. Some of the noise measurements are shown in Figure 1 and Figure 2. There is a very clear gain in going from the smallest FET to the one actually used in the amplifier. The results suggest that a reduction in white noise by about 15% could be achieved by doubling the input
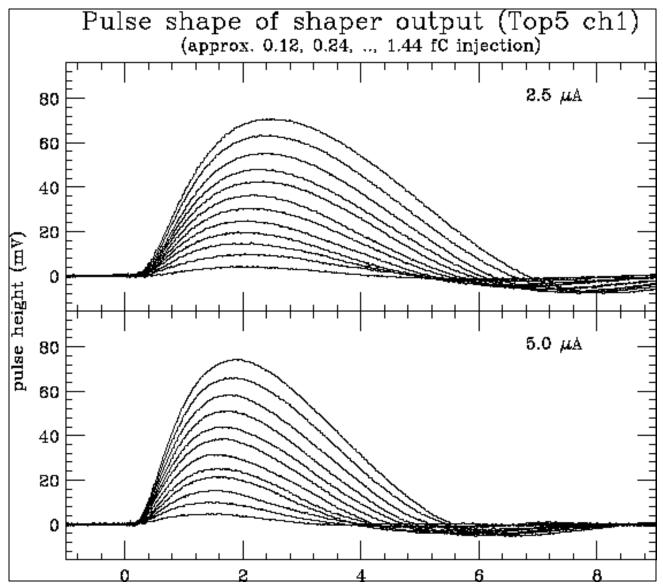

Figure 3. Pulse shapes measured with a Model-28 PicoProbe at the shaper output, under two bias conditions.

FET size, but most, if not all, of that noise gain would be lost by increased input capacitance for the input FET.[2]

5   Top5 Test-Chip Measurements

The "Top5" test chip included three amplifier-discriminator channels.   Its noise was measured by two methods, first with a spectrum analyzer attached to a Pico-Probe on the internal pads at the amplifier outputs, and second by charge-injection scan.   Figure 3 shows pulse shapes measured at the shaper output under the two bias conditions studied:

1. SLOW: 2.5 µA at the IBIAS input, from which all internal bias currents (except the input FET current) are derived. This is as in configuration 1 of the simulations, but keep in mind that the time constants do not match well between measurement and simulation even though the bias is the same.

2. FAST: 5.0 µA at the IBIAS input, and 96.5 nA current subtracted from node TILOW, as in configuration 3 of the simulations.

The gains inferred from Figure 3 are not linear, but the peak pulse heights fit well to the following quadratic curves:

- pulse height = $0.968 + 34.85 \times Q + 10.44 \times Q^2$ for 2.5 µA bias,

- pulse height = $1.236 + 35.34 \times Q + 11.81 \times Q^2$ for 5.0 µA bias.

From these results we infer a gain at 0 fC input charge of close to 35 mV/fC for both bias conditions. This contrasts with about 55 mV/fC gain at 1 fC input charge, obtained by taking the derivative at 1 fC.

As can be seen in Table 1, the gains and time constants do not agree well between measurement and simulation. In fact, since the gain is defined by the peak of the shaper output, it is highly correlated with the time constants.

---

[2] For reference, the BTEM amplifiers used a width of 2500 µm and length 1.2 µm.
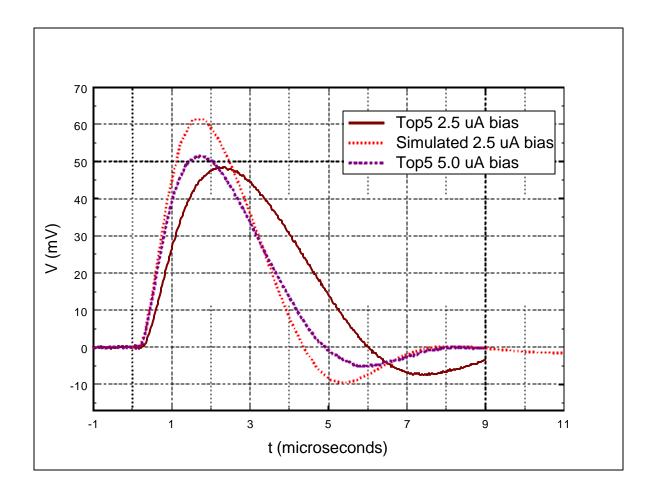
Figure 4. Comparison of measured and simulated shaper output pulses for 1 fC input charge.

5.1 Spectrum Analyzer

A Model-28 PicoProbe with a factor of 20 attenuation and 50Ω output impedance was connected directly to the input of the HP 4195A spectrum analyzer. With the probe on the internal pad and the amplifier powered, the noise was measured from 10 kHz to 3 MHz and averaged over 100 measurements. The measurement was repeated with the probe lifted off of the pad and the Top5 chips powered off, to get the background noise generated by the measurement system. The background noise was then subtracted in quadrature from the measurement taken with the probe on the pad. The results from the preamp output and the shaper output are plotted in Figure 5 for both bias conditions. Note that a normalization error in the background subtraction cannot explain the excess low-frequency noise seen at the shaper output, as the background spectrum does not exhibit such a sharp increase to low frequency. Our evidence indicates that this flicker noise really is generated in the shaper. (The preamp also generates such flicker noise, as seen in Figure 5, but it clearly gets largely filtered out by the AC coupling to the shaper—the differentiation of the pulse shaping.) The simulation was done without any flicker noise at all, but the contribution of the low-frequency rise to the noise integral is negligible, anyway.

The rms noise integral at the shaper output is calculated by squaring the background-subtracted spectrum at the shaper output bin-by-bin, adding together the squared values, and taking the square root. The results are 5.6 mV for 2.5 µA bias and 6.6 mV for 5.0 µA bias. This can be converted to an equivalent noise charge (ENC) by dividing by the gain in units of mV/fC. If we use as the gain the pulse height at 0 fC charge injection (which is appropriate, since the noise consists of small fluctuations around zero), then the ENC values are 1000 electrons and 1170 electrons, respectively.[3]   These ENC values are appropriate for comparison with the direct measurement of ENC obtained in Section 5.2, since the definition is consistent in the two cases.
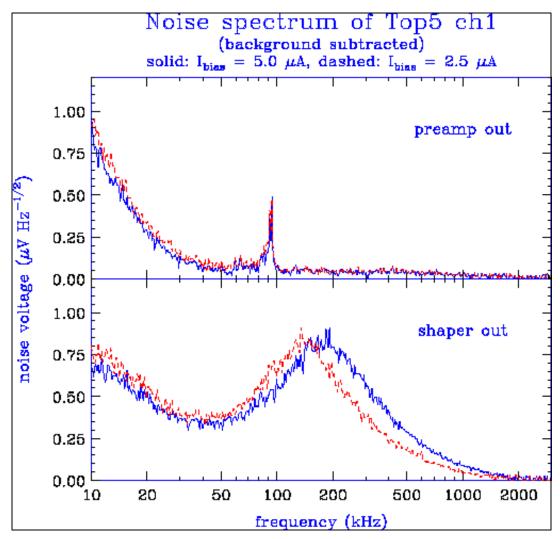
Figure 5. The noise spectrum measured on internal pads of the Top5 chip at the preamp and shaper output nodes. The vertical scale must be multiplied by 20 to correct for the PicoProbe attenuation. (The large spike in the preamp spectrum is from an external source, such as a switching power supply.)

[3] These ENC values are misleading because, due to the large nonlinearity, one cannot simply use them to calculate a signal-to-noise value in the usual way, by dividing the signal in electrons (i.e. for a MIP) by the ENC.

Table 1. Spice simulation results and Top5 measurements. The simulated gains were calculated for a 0.1 fC input charge.

Config.	Peaking Time at the Shaper Output	Small-signal gain at shaper output (mV/fC)	Small-signal gain at comp. Input (mV/fC)	Noise at the Shaper Output (mV rms)	Noise at the Comparator Input (mV rms)	ENC at the shaper output (electrons)	ENC at the comparator input (electrons)
1 sim.	1.7 μs	50.0	22.2	11.0	7.09	1370	1990
2 sim.	1.7 μs	51.5	43.5	11.6	10.9	1406	1560
3 sim.	1.3 μs	52.5	26.6	12.8	9.09	1520	2130
4 sim.	1.3 μs	53.4	45.1	12.8	12.7	1500	1760
1 meas.	2.3 μs	34.9	(no pad)	5.6		1000	1450
3 meas.	1.7 μs	35.3	(no pad)	6.6		1170	(not meas.)

5.2 Charge-Injection Scan

The ENC at the comparator input was also measured directly for the 2.5 μA bias of the Top5 chip by means of a charge injection scan. The threshold was set to about 2.2 fC, and charge was injected by means of a small voltage step applied to a 45 pF external capacitor attached to the amplifier input. The value of injected charge was stepped across the threshold region, and for each value of injected charge the efficiency for the comparator to fire was measured on the basis of 1000 applied input pulses. The resulting threshold efficiency curve was fit to an error function (or equivalently, differentiated and then fit to a gaussian) to extract the rms noise. The result is an ENC of 0.232 fC or 1450 electrons. The ratio of this value to the ENC at the shaper output, measured from integrating the noise spectrum, agrees well with the same ratio from the simulation (first row of Table 1).

6 Discussion of Results

The differentiation time constant for the AC coupling from shaper to comparator in the Top5 chip is too short, resulting in a significant deterioration of signal-to-noise represented by the 45% increase in ENC from the Spice simulations shown in Table 1. The same simulations show that the effect should be only about 10% in the GTFE64d chip, for which the relevant time constant was increased by about a factor of 10.

The two different noise measurements done for the 2.5 μA bias are in good agreement and support each other. The integration of the noise spectrum at the shaper output gives an ENC of 1000 electrons, where the gain at zero input charge is used to translate noise voltage at the shaper output to equivalent input charge. The charge-injection scan measures the noise on top of a 2.2 fC input pulse, for which the amplifier gain (and hence the amplification of the input FET noise) is about 24% higher than at zero input charge. However, the method of scanning the input charge and fitting the resulting threshold curve gives directly the ENC value, in this case 1450 electrons. This is 44% higher than at the shaper output, which is consistent with the 45% higher ENC at the comparator input that was found in the simulations.

As a sanity check, the $4 \text{ nV}/\sqrt{\text{Hz}}$ voltage noise of the input FET itself, with no differentiation in the shaping but with a t=2 μs integration time constant, would give an ENC of 830 electrons with a $C_d = 47 \text{ pF}$ input load plus $C_{\text{FET}} \approx 2 \text{ pF}$ for the FET itself, from the formula

$$\text{ENC} \approx \frac{1}{e} \cdot \left(C_d + C_{\text{FET}}\right) \cdot \sqrt{V_n^2 \frac{F}{t}} \text{ with } F\text{=}0.92 \text{ for an ideal CR/RC shaper}$$

The rest of the amplifier can be expected to add about another 20% of noise, so the measured ENC values at the shaper output are reasonable.

As seen in Table 1, the simulated ENC is about 40% greater than the measured. This discrepancy is puzzling, as the difference in integration times can only explain about a 20% effect at most, and the noise level used in the simulation for the input FET agrees well with our measurements. The simulated ENC is also high relative to the above analytical calculation. However, the calculation applies to a CR/RC shaper with equal integration and differentiation time constants, while the differentiation time constant in the simulation at low input levels is clearly quite a bit shorter than the integration time constant. This can be corrected by adjusting the bias. Figure 6 shows the simulated shaper output pulse for the default bias (2.5 μA) and for a bias point adjusted to make it look similar to an ideal pulse of the form $te^{-t/t}$, with t=2 μs, for which the analytical formula should be applicable. The required adjustment is to increase the bias current to 3.0 μA and to add a 5.25 MΩ resistor from TILOW to ground. A small 0.1 fC input signal is used, because the shaper only resembles an ideal RC/CR filter at low amplitudes. Figure 7 then shows the simulated noise spectrum for each case. The rms noise integral for the adjusted configuration is 14.0 mV, and the small-signal gain is 86.3 mV/fC, leading to an ENC value of 1010 electrons, which is quite consistent with the analytical formula, assuming that the rest of the amplifier, beyond the input FET, contributes about 20% to the noise.[4]

---

[4] This is about right, with most of the extra 20% coming from the current source in the folded-cascode preamp input stage.
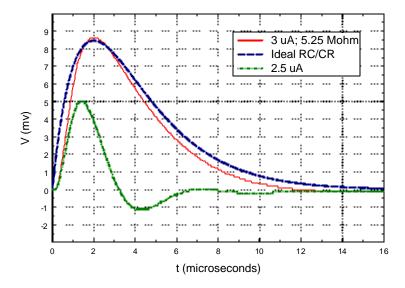
Figure 6. **Simulated shaper output pulses for two bias configurations and 0.1 fC input charge, compared with an ideal RC/CR pulse.**

The ENC results shown in Table 1 can be misleading (suggesting more S/N than is really there), because they do not take into account the fact that the gain increases significantly with increasing input signal level. Nevertheless, the results suggest that the design does have adequate noise margin, given that we would like to run with about a 1.0 to 1.5 fC threshold (6000 to 10000 electrons), which should be at least 4σ above the noise level. Still, the most relevant test of the noise performance is obtained by actual measurements of noise occupancy versus threshold in a many-channel system, which will be possible with the recently fabricated GTFE64d chip. Noise occupancy is the relevant quantity (not ENC) as far as operational performance is concerned, and by measuring noise occupancy one avoids the whole issue of how the amplifier nonlinearity affects the interpretation of ENC numbers and signal-to-noise. That is why the Tracker requirements are stated in terms of noise occupancy and why occupancy measurements are specified as the means of verification of the noise performance.
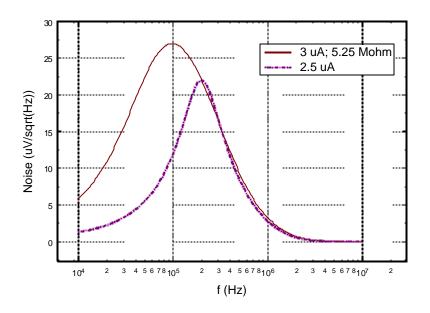
Figure 7. Simulated noise spectra for two bias conditions.

Top level of the test schematic.

INS
IAC

IDC
2.5UA

38K
RBIAS

INPT

CHAN

INPT

BIAS0
SUB
CAL

CL
47PF

CAL
BIAS

BIAS[0:11]
BIAS[0:11]

BIAS[0:11]
BIAS[0:11]

BIAS10

BIAS3

THRESH

C?
0.01UF

AVDD2
SOUT1

666

1K
R?

AVDD

L8
555

20MV
VPULSE

VRC

AGND

IBIAS

AVDD

ILOW

AVDD

AGND

AVDD2

OUTPT

OUTPUT

0.05V
DC

AGND

999MEG R?

2.5V
DC

0V
DC

1.5V
DC

GND

0.5V
DC

BIAS[0:11]

A or X 1

AVDD
VRC
ILOW
IBIAS
AGND

1.5 ua   500 nA   500 nA   100 nA   500 nA   500 nA   100 nA   500 nA   500 nA   2 * 500 nA   BIAS[0:11]

MP11   MP12
W=1.8U L=9U

MP31
W=1.8U L=9U

MP14   AVDD
W=1.8U L=9U

MP13
W=1.8U L=9U   M=5

MP15
W=1.8U L=9U

MP17
LH

MP16
W=1.8U L=9U   M=2 (VP)

LG

LN

MN11
W=1.8U L=1.8U
BULK=AGND   M=5

MN12
W=1.8U L=1.8U   M=3
BULK=AGND

MN13
W=1.8U L=1.8U
BULK=AGND

MN14
W=1.8U L=1.8U
BULK=AGND

MN17
W=1.8U L=1.8U
BULK=AGND   M=5

MN15
W=1.8U L=1.8U
BULK=AGND

MN16 MN61
W=.9U L=4.5U
BULK=AGND

MN31
W=30U L=9U
BULK=AGND

IBIAS
IBIAS

BIAS1
BIAS4 (VRS)
BIAS8 (VPB)
BIAS6 (VN)
BIAS0(VI1)   37 uA
BIAS11 (VCLO)

100 nA
VRC   2.5 ua
ILOW

20nA   4nA   20nA   20nA   20nA   0.16nA

MP18
W=1.8U L=9U

MP19
W=1.8U L=9U   M=5

MP1A
W=1.8U L=9U   M=5

MP1B
W=1.8U L=9U   M=5

MP32
W=1.8U L=1.8U   M=1

MP1C
W=1.8U L=9U   M=9

MP1D
W=1.8U L=9U   2.2nA

MP1G
W=1.8U L=9U

MN18
W=1.8U L=1.8U
BULK=AGND

MN19
W=1.8U L=1.8U
BULK=AGND   M=5

MN1A
W=1.8U L=1.8U
BULK=AGND   M=5

MN1B
W=1.8U L=1.8U   M=5
BULK=AGND

MN1C
W=1.8U L=1.8U
BULK=AGND

MN1D
W=1.8U L=1.8U
BULK=AGND

ILOW
ILOW

L7   L4

AVDD   20nA

BIAS2 (VIR)
BIAS9 (VPL0)
BIAS5(VSL0)
BIAS7 (VHLF2)

A or X 1

BIAS[0:11]

BIAS[0:3]

BIAS[4:7]

BIAS[8:10]

AVDD   RST   AVDD

VDD   PLSE
VCLD RST
ARESET5   R
AGND GATE
AGND
GATE

SOUT1

THRESH

BIAS[8:10]
IP   LB
COMPARATOR5
IM   AGND
AVDD
Pad driver is omitted here

LB

AGND

c

GATE

GATE

C13
386FF
AGND

C?
60FF

BIAS[4:7]
SIN   SAGND
SHAPER5 GATE
IT
AVDD
AGND
AVDD
AGND
AVDD

BIAS4

L1 C1772FF
2
1

DRV
V BIAS
I fold G
IP
POUT

AVDD

AGND

AVDD2

RST
RST   OUT
AVDD2

BIAS[0:3]
IN P OUT
PREAMP5
AGND AVDD
AGND
AVDD

INPUT

CTEST
.046P

CAL

SUB

page 21

APPV'D
DATE
APPV'D
DATE
APPV'D
DATE
APPV'D
DATE

APPV'D
DATE
APPV'D
DATE
APPV'D
DATE
APPV'D
DATE

AVDD

2.5V

C1
0.102P

1.6741V

BIAS2

160 pA

MP12   AVDD

W=1.8U
L=9U

BIAS1

1.5 uA

MP13   AVDD

W=1.8U
L=9U

0.102P

C2

1.0491V

C13=.4P: 1/e at 400 ns
C13=.8P: 1/e at 580 ns

OUT

A   gm=8E-5

MN2
W=30U
L=6U
AD=50P
AS=50P
PD=63U
PS=63U

(z e r o   b i a s)
Cs=110fF

MP51   AVDD

W=.9U
L=4.5U

AGND

gm=2E-9
R=500Meg
tau=130us

C4
0.386P

C3
0.13P

36 uA

MP1
W=124.2U
L=1.2U
AD=112P
AS=112P
PD=126U
PS=126U
NRD=.000159
NRS=.000159
M=-12

L2

gm=9E-4
Cg=15pF

0.5897V

(QVDD)

30 pA

0.6120V

MN37

W=30U
L=9U
BULK=AGND

Cs=110fF
(z e r o   b i a s)

C5
0.102P

MN62
W=.9U
L=4.5U
BULK=AGND

0.4510V

RST

AVDD2

IN

BIAS3

BIAS0

MN61
W=.9U
L=4.5U
BULK=AGND
M=2

AGND

exp.gm13=.9E-2*SQRT(35*2800E-6) = 2.8E-3
exp.tau-rise= .8 * --------- = 90 ns
                   .60E-12

                   .13 9E-4

APPV'D
DATE

APPV'D
DATE

APPV'D
DATE

APPV'D
DATE

APPV'D
DATE

APPV'D
DATE

APPV'D
DATE

500nA

$W = 1.8U$
$L = 9U$

MP1

V $2.5V$

BIAS $1.2101V$

A

0

MP3
$W = 1.8U$
$L = 1.8U$

AS=7P
AD=7P
PS=11U
PD=11U

$gm = 64E-7$
$R = 160K$

I

G

S or X3

page 24

BIAS[4:7]

Total = 1.5 uA (was 13 uA)

Original: 3uA   Original: 2*16nA   Original: 7.5uA   2.6uA

SCIPP
Santa Cruz Institute
for Particle Physics

TITLE: SHAPER5_OLD

DATE: 4-19-2001-13:59   DRAWN BY: D. Freytag (SLAC)

University of California at Santa Cruz

TAUint = (160+190)K * 1.66P = 580 ns

TAUdiff = 20Meg*.05P = 1000 ns

R = (.3+.07)P / .05P*38E-6 = 190K

gm = 38E-6
Cg = 330ff

gm = 1E-7

gm = 1E-7
R = 2*10Meg

MP4A
W = 24U
L = .9U
AS=80P
AD=80P
PS=56U
PM=4

MP4B (zero bias
W = 24U   Cd=60ff
L = 12U
AS=80P
AD=80P
PS=56U
PD=56U

MN62
W = .9U
L = 4.5U
BULK=AGND

MN4
W = 1.8U
L = .9U
BULK=AGND

MN62
W = .9U
L = 4.5U
BULK=AGND

MP14
W = 1.8U
L = .9U

MP13
W = 1.8U
L = .9U

MP12
W = 1.8U
L = .9U

MP11
W = 1.8U
L = .9U

MN11
W = 1.8U
L = 1.8U
BULK=AGND

MN61
W = .9U
L = 4.5U
BULK=AGND
M = 5

(zero bias)
Cd = 10ff

AVDD

AVDD

AVDD

2.3731V

2uA

6.7nA

0
0.6643V

1.6195V

1.8670V

2.5V

0V

L3

L6

J

L4

L5

C6
.046P

C5
.386P

C3
.102P

C4
.102P

C2
.102P

C1
.102P

AVDD
2.5V

1.2101V
BIAS4

1.5274V
BIAS5

1.25V
BIAS7

I

GATE

AGND

.9649V
BIAS6

.102P

C or X9

Total = 1.5 uA (was 5.5 uA)
Orginal: 3.8 uA

1.7 uA

1.7 uA

.5uA

1 uA

2.5V

C1
BIAS[8:10] 102FF

BIAS8
1.2101V

Input transistors doubled
up to symmetrize geometry

2.3682V

2.3537V

Circuitry to restore REF to VREF

MP35
C4
102FF
W=1.8U
L=1.8U

AVDD

MP34
W=1.8U
L=1.8U
M=4

MP21
W=.9U
L=.6U

L3

MN17
W=1.8U
L=1.8U
BULK=AGND

L4

MP33
W=1.8U
L=1.8U

MP32
W=1.8U
L=1.8U

MP31
W=1.8U
L=1.8U

L0

L6

L7

O

MN14
W=1.8U
L=1.8U
BULK=AGND

MN13
W=1.8U
L=1.8U
BULK=AGND

L5

MP2
W=3U

MP1
W=3U

L1

M=2
AD=7P
AS=7P
PD=11U
PS=11U

M=2
AD=7P
AS=7P
PD=11U
PS=11U

W=1.8U
L=1.8U

W=1.8U
L=1.8U

MN12
W=1.8U
L=1.8U
BULK=AGND

L8

MN46
W=1.8U
L=.9U
BULK=AGND

L2

MN45
W=1.8U
L=.9U
BULK=AGND

C5
386FF

C3
102FF

BIAS9

BIAS10
(VREF)

C2
102FF

MN11
W=1.8U
L=1.8U
BULK=AGND

AVDD

IM
1.3650V

AGND

IP

GATE

STANFORD LINEAR ACCELERATOR CENTER
U.S. DEPARTMENT OF ENERGY
STANFORD UNIVERSITY   STANFORD, CALIFORNIA

GLAST Front-End Readout Chip (GTFE64)
Version D   GLAST Project
Drawn by COMPARATOR5_2

7-6-2001-14:47

B

SHEET 2 OF

DATE   APPROVALS

ENGR
DFTR
CHKR

APPV'D
DATE

APPV'D
DATE

APPV'D
DATE

APPV'D
DATE